

1 ABSTRACT OF THE DISCLOSURE

2 Memory integrated circuitry includes an array of memory cells
3 formed over a semiconductive substrate and occupying area thereover,
4 at least some memory cells of the array being formed in lines of active
5 area formed within the semiconductive substrate which are continuous
6 between adjacent memory cells, said adjacent memory cells being
7 isolated from one another relative to the continuous active area formed
8 therebetween by a conductive line formed over said continuous active
9 area between said adjacent memory cells. At least some adjacent lines
10 of continuous active area within the array are isolated from one another
11 by LOCOS field oxide formed therebetween. The respective area
12 consumed by individual of said adjacent memory cells is ideally equal
13 to less than $8F^2$, where "F" is no greater than 0.25 micron and is
14 defined as equal to one-half of minimum pitch, with minimum pitch
15 being defined as equal to the smallest distance of a line width plus
16 width of a space immediately adjacent said line on one side of said
17 line between said line and a next adjacent line in a repeated pattern
18 within the array. The respective area is preferably no greater than
19 about $7F^2$, and most preferably no greater than about $6F^2$.

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